IN THE CLAIMS

Please amend the following claims.

Claims 1-10 (cancelled)

11. (currently amended) A method of making a junction, comprising:

a) forming a gate electrode on a surface of a substrate, the substrate being of a first conductivity type;

b) isotropically etching the substrate such that a recess in the substrate is formed, the recess including a portion that underlies the gate electrode, the recess having a surface;

c) selectively forming a layer of a first material having the first conductivity type over the surface of the recess, and within ~~including~~ the portion of the recess that underlies the gate electrode; and

d) selectively forming a layer of a second material having a second conductivity type over ~~the surface of the recess,~~ and within ~~including~~ the portion that underlies the gate electrode.

12. (cancelled)

13. (currently amended) The method of Claim 11 [[12]], wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon, and the second material comprises doped silicon.

14. (currently amended) The method of Claim 11 [[12]], wherein the substrate comprises silicon doped to have the first conductivity type; the first material comprises doped silicon germanium, and the second material comprises doped silicon germanium.

15. (previously presented) The method of Claim 14, wherein the first material has a thickness that is less than a thickness of the second material.

16. (previously presented) The method of Claim 15, wherein the second material has a top surface that is above a plane defined by the surface of the substrate.

17. (original) The method of Claim 11, wherein the patterned structure comprises a dielectric layer and a conductive material disposed over the dielectric layer.

18. (original) The method of Claim 11, wherein etching passivates the surface of the recess.

19. (original) The method of Claim 11, wherein etching comprises exposing the substrate to SF_6 and He in an RF plasma etching system.

20. (original) The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material.

21. (original) The method of Claim 11, wherein forming the first material comprises epitaxially depositing a layer of crystalline material; and forming the second material comprising epitaxially depositing a layer of crystalline material; wherein the substrate remains unexposed to the atmosphere subsequent to forming the first material and prior to forming the second material.

22. (currently amended) A method of making a transistor, comprising:

forming a dielectric on a first surface of a wafer;

forming a conductive layer overlying the dielectric;

patterning the conductive layer to form a gate electrode and patterning the dielectric so as to form a gate dielectric ~~structure~~;

forming recesses adjacent and partially subjacent the gate dielectric and gate electrode ~~structure~~; and

in a continuous operation, back filling the recesses with doped crystalline material[[;]] , wherein back filling comprises forming crystalline material of at least a first conductivity type within a portion of the recess partially subjacent the gate dielectric and gate electrode.

23. (original) The method of Claim 22, wherein the crystalline material of the first conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.

24. (currently amended) The method of Claim 22, wherein back filling further comprises forming crystalline material of a second conductivity type within the portion of the recess partially subjacent the gate dielectric and the gate electrode.

25. (original) The method of Claim 22, wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium.

26. (original) The method of Claim 25, wherein back filling comprises a selective deposition.

27. (currently amended) A method of fabricating a FET, comprising:

forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type;

forming first spacers along the sidewalls of the gate electrode;

forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface;

substantially filling the recess ,including the portion underlying the gate electrode, with a first layer of doped crystalline material, the first layer having a second conductivity type.

28. (original) The method of Claim 27, further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate.

29. (original) The method of Claim 27, further comprising forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess.

30. (original) The method of Claim 29, wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power in the range of approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium.